gate electrode layer **424** is formed of tantalum or titanium containing materials such as TaC, TaN, TiN, TaAlN, TaSiN, and combinations thereof. These metal-containing materials may be in the form of metal carbides, metal nitrides, or conductive metal oxides. Other embodiments may utilize other types of metals, such as W, Cu, Ti, Ag, Al, TiAl, TiAlN, TaCN, TaSiN, Mn, WN, Ru, and Zr. The formation methods of the gate electrode layer **424** include ALD, PVD, metal-organic chemical vapor deposition (MOCVD), and the like.

FIG. **4** illustrates a gate electrode layer **424** having a single metal layer for illustrative purposes only and may include two or more layers for a composite gate structure. For example, the gate electrode layer **424** may be adjusted to exhibit a work function suitable to the type of device being formed, e.g., a PMOS device or an NMOS device. Generally, it may be desirable to adjust the work function of the gate electrode to the band-edge of the silicon; that is, for an NMOS device, adjusting the work function close to the conduction band, and for a PMOS device, adjusting the work function close to the valence band. In some embodiments, multiple layers may be used to adjust the work function and other operating characteristics of the device.

FIG. **5** illustrates results of removing excess materials of the interfacial layer **420**, gate dielectric layer **422**, and the gate electrode layer **424** using, for example a CMP process.

Thereafter, further processing may be performed. For example, a second ILD layer may be formed over the first ILD layer, metallization layers including conductive lines, vias, and dielectric layers may be formed, passivation and contact structures may be formed, and singulation and/or packaging processes may be performed.

FIG. **6** is a flow diagram illustrating process steps to form an open profile gate electrode in accordance with some embodiments. The process begins in step **602**, wherein a substrate is provided with a dummy gate stack formed thereon. The dummy gate stack has spacers formed along sidewalls of the dummy gate stack. The spacers may include one or more spacer layers. For example, in an embodiment, the spacer layers include a plurality of dielectric layers having different etch rates, such as a silicon oxide layer and a silicon nitride layer. Additionally, an ILD layer may be formed over the dummy gate stack and planarized to expose an upper surface of the gate stack.

In step **604**, the dummy gate stack is removed and a funnel-shaped opening is formed. In an embodiment, the etch process uses a dry etch such that the spacer layers etch at different rates. As a result of the different etch rates, a funnel-shaped opening may be created.

Thereafter, in step **606**, a gate stack may be formed in the funnel-shaped opening, thereby forming a gate electrode having an open profile. The gate stack may include, for example, an interfacial layer, a gate dielectric layer, and a gate electrode. In some embodiments, the gate electrode includes one or more metal layers, and may include a metal work function layer.

In an embodiment, a method of forming a semiconductor device is provided. The method includes providing a substrate and forming a gate stack and gate spacers adjacent the gate stack. A first dielectric layer is formed over the substrate adjacent the gate spacers. The gate stack and upper portions of the gate spacers are removed, thereby forming a funnel-shaped opening. A gate electrode is subsequently formed in the funnel-shaped opening.

In another embodiment, another method of forming a semiconductor device is provided. The method includes providing a substrate, wherein the substrate has a dummy gate stack formed thereon with one or more first dielectric layers along sidewalls of the dummy gate stack. The gate stack and at least a portion of the one or more first dielectric layers are removed, thereby forming a funnel-shaped opening. A gate electrode is subsequently formed in the funnel-shaped opening.

In yet another embodiment, a semiconductor device is provided. The semiconductor device includes a substrate. The substrate has an overlying dielectric layer, wherein the dielectric layer has a funnel-shaped opening. A gate electrode is positioned in the funnel-shaped opening.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of forming a semiconductor device, the method comprising: providing a substrate forming a gate stack and gate spacers adjacent the gate stack; forming a first dielectric layer over the substrate adjacent the gate spacers; removing the gate stack and upper portions of the gate spacers, thereby forming a funnel-shaped opening, the funnel-shaped opening exposing a semiconductor material of the substrate between the gate spacers; and forming a gate electrode in the funnel-shaped opening, wherein the funnel shaped opening comprises a funnel slope of about 30° to about 45° relative to a major surface of the substrate.

2. The method of claim **1**, wherein the forming the gate stack and the gate spacers comprises forming a first dielectric spacer adjacent the gate stack and a second dielectric spacer adjacent the first dielectric spacer, the first dielectric spacer being formed of a different material than the second dielectric spacer.

3. The method of claim **2**, wherein the first dielectric spacer has a different etch rate than the second dielectric spacer.

4. The method of claim **2**, wherein the first dielectric spacer comprises a silicon oxide and the second dielectric spacer comprises a silicon nitride.

5. The method of claim **1**, wherein the removing comprises:

performing a first etch process having a first ratio of an etch rate of the gate stack to an etch rate of the gate spacers; and

performing a second etch process having a second ratio of an etch rate of the gate stack to an etch rate of the gate spacers, the second ratio being greater than the first ratio.

6. The method of claim **5**, wherein the first ratio is from about 1.2 to about 1.5.

7. A method of forming a semiconductor device, the method comprising: providing a substrate, the substrate having a dummy gate stack formed thereon with one or more first dielectric layers along opposing sidewalls of the dummy gate stack; removing the dummy gate stack between the one or more first dielectric layers along opposing sidewalls of the dummy gate stack and at least a portion of the one or more first dielectric layers and exposing the substrate,